#18/D 7/25/03 JJ

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Mitsuo Zen

Application No.: 09/868,573 Art Unit: 1725

Filed: August 20, 2001 Examiner: L. Edmondson

For: SOLDER COATED MATERIAL
AND METHOD FOR ITS MANUFACTURE



RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action mailed on April 21, 2003, the Applicant requests reconsideration of the rejections of the claims in view of the following remarks.

Rejection 1

In paragraph 1 of the Official Action, claims 16 - 23, 25, 27, 28, 30, 34, and 39 were rejected under 35 USC 102(b) as anticipated by McAndrew (U.S. Patent No. 6,095,404). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated

layer. Independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer. Independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. McAndrew does not disclose such products or such a method.

McAndrew discloses a method for assembling electronics in which a thick layer of solder of approximately 500 micro-inches is applied by electroplating or dipping atop copper and nickel layers on a printed wiring board. The bulk of the solder is then removed by heating the solder to oxidize it and turn it to ash, leaving a very thin solderable layer. Components can then be attached to the solderable layer by conventional techniques. Columns 1 and 2 of McAndrew disclose that the copper and nickel layers can be formed by plating, but there is no disclosure of what methods of plating (such as electroplating, electroless plating, or mechanical plating) are either suitable or intended, and the only mention of electroplating in McAndrew is with respect to a method of forming a solder layer, as an alterative to dipping.

Thus, McAndrew does not disclose a hot dip solder plating layer on an electroplated layer, so it does not disclose all the features of claims 16, 20, or 25 and cannot anticipate these claims or claims 17 - 19, 21 - 23, 27, 28, 30, 34, and 39 which depend therefrom. These claims are thus allowable.

Claims 17, 21, and 27 further patentably distinguish the present invention from McAndrew. These claims state that the

substrate on which an electroplated layer is provided is an iron-nickel alloy. The only substrate which is treated in McAndrew is a printed wiring board, and there is no disclosure or suggestion of forming an electroplated layer on an iron-nickel alloy. The Official Action mistakenly refers to column 4, lines 53 - 59 of McAndrew as supposedly teaching an iron-nickel alloy substrate, but what this passage actually states is that the solder layer of McAndrew works well when the leads of external components being subsequently attached to the resulting printed wiring board of McAndrew have a nickel/iron content such as alloy 42 There is no suggestion in McAndrew of forming an electroplated layer on a nickel/iron substrate, and thus no disclosure or suggestion of the features of claims 17, 21, and 27.

Claims 19 and 23 further patentably distinguish the present invention from McAndrew. These claims state that the material having excellent solderability which is electroplated on a substrate is a tin-silver alloy. The Official Action cites column 2, lines 30 - 38 of McAndrew as supposedly teaching an Sn-Ag alloy as a plated layer on which solder is applied, but this reliance on McAndrew is incorrect. This passage of McAndrew describes various solders which have been used in the past as a top layer atop a plating system. Not only is the Sn-Ag solder described in this passage used for a different purpose from the "material having excellent solderability" in claims 19 and 23, but it is also an alloy which the inventive alloy of McAndrew is intended to replace, since a Sn-Ag solder is described as being brittle and having an affinity for copper. Thus, McAndrew

nowhere discloses or suggests a tin-silver alloy as an electroplated material having excellent solderability, as set forth in claims 19 and 23.

Rejection 2

In paragraph 2 of the Official Action, claims 16, 18 - 20, 22, 23, 25, 26, 28 - 30, 34, 39, and 40 were rejected under 35 USC 102(b) as anticipated by Tadauchi et al (U.S. Patent No. 6,123,248, referred to below as Tadauchi). This rejection is respectfully traversed.

As discussed above, independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer atop a substrate of a difficult to solder material, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer on a substrate of a difficult to solder material, and independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. Tadauchi does not disclose such products or such a method.

Tadauchi describes a soldering apparatus and method which imparts oscillatory wave energy to a solder and a base material being dipped into the solder. One type of base material to which solder can be applied is a printed circuit board having wiring formed on an insulating substrate. Example 2 of Tadauchi (columns 16 and 17) describes an example of forming solder with a thickness of 15$\mu$m on laminated wiring of copper 18$\mu$m/nickel

5μm/gold 0.05μm.

The Official Action states that Tadauchi teaches electroplating a layer of material having excellent solderability on a substrate comprising Ni with the plated layer being 0.5 μm. This statement is incorrect. There is no suggestion in Tadauchi that any of the layers forming the laminated wiring are electroplated. Furthermore, the Official Action has misstated the thickness of the Au layer. It is 0.05 μm, not 0.5 μm. In addition, the Official Action appears to be saying that the 5μm nickel layer in Tadauchi corresponds to the "substrate comprising a difficult to solder material" in claims 16, 20, and 25, but nickel in fact has excellent solderability and is not a "difficult to solder material".

Therefore, since Tadauchi does not disclose a hot dip solder plating layer on an electroplated layer atop a substrate of a difficult to solder material, it does not disclose all the features of claims 16, 20, or 25 and cannot anticipate these claims or claims 18, 19, 22, 23, 26, 28 - 30, 34, 39, and 40 which depend therefrom. These claims are thus allowable.

Claims 19 and 23 further patentably distinguish the present invention from Tadauchi. These claims state that the material having excellent solderability which is electroplated on a substrate is a tin-silver alloy. Tadauchi does not disclose or suggest such a feature. The Official Action points out that column 4, line 65 and column 17, lines 30 - 55 of Tadauchi mention Sn-Ag alloys. However, both of these passages refer to a solder to be applied by hot dipping and having nothing to do with

the electroplated base plating being described by claims 19 and 23. These claims are therefore not anticipated.

Rejection 3

In paragraph 3 of the Official Action, claims 16, 18, 20, 22, 25, 28, and 30 were rejected under 35 USC 102(b) as anticipated by Siemens AG (DT 2340423 A, referred to below as Siemens). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer, and independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. Siemens does not disclose such products or such a method.

Siemens discloses a multilayer structure including a plurality of metal layers formed by electroless plating atop a substrate (such as a silica substrate) and a dipped solder layer formed atop the plated layers. Siemens is very specific that the plated layers are formed by electroless plating, and nowhere is there any suggestion of forming the plated layers by electroplating. Thus, Siemens does not disclose a hot dip solder plating layer on an electroplated layer, so it does not disclose all the features of claims 16, 20, or 25 and cannot anticipate these claims or claims 18, 22, 28, and 30 which depend therefrom. These claims are thus allowable.

Rejection 4

In paragraph 4 of the Official Action, claims 16, 18 - 20, 22, 23, 31, 34, 35, 39, and 40 were rejected under 35 USC 102(b) as anticipated by Izuta et al (U.S. Patent No. 5,609,287, referred to below as Izuta). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, and independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer. Izuta does not disclose such products.

Izuta discloses a semiconductor device in which a semiconductor chip is joined to another member by a plurality of layers of solder. As shown in Figure 1 and described in column 7, lines 8 - 36, a second solder 5a and 5b is applied to opposite sides of a first solder 4 by gilding. The solder layers 4, 5a, and 5b are sandwiched between a semiconductor chip 1 and a copper lead frame 2, and heating is carried out to melt the second solder 5a and 5b but not the first solder 4. The dictionary defines "gild" as "to overlay with a thin layer of gold", so it is not clear to what process this term refers to in Izuta, but there is no indication that the second solder 5a and 5b is applied by electroplating. There is also clearly no hot dip solder plating layer. The first solder 4 is a preform, and together with the second solder 5a and 5b it defines a larger preform for joining the chip 1 and the lead frame 2.

Thus, since Izuta does not disclose either an electroplated

layer or a hot dip solder plating layer, it fails to disclose all the features of claims 16 and 20 and cannot anticipate these claims or claims 18, 19, 22, 23, 31, and 34 which depend therefrom. These claims are accordingly allowable.

Regarding dependent method claims 35, 39, and 40, since the Official Action does not contain a rejection of independent method claim 25 from which these claims depend, and since a dependent claim cannot be anticipated unless the parent claims is also anticipated, the rejection of the dependent claims is defective on its face. These claims are therefore allowable.

Rejection 5

In paragraph 5 of the Official Action, claims 16 - 24, 31, 43, and 44 were rejected under 35 USC 102(b) as anticipated by Miyahara (U.S. Patent No. 5,629,559). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, and independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer. Miyahara does not disclose such products.

Miyahara discloses a package for a semiconductor device including a ground layer, a power layer, and a signal layer separated from each other by insulating layers. According to the Official Action, column 7, lines 13 - 40 of Miyahara disclose electroplating a layer of material having excellent solderability such as Ni, Cu, or Au, but the passage cited by the Official

Action is a description of materials which can be used for the power layer, the ground layer, or the signal layer, and the Applicant cannot find any description of these layers being formed by electroplating or any other form of plating. On the contrary, in Example 1, a power layer and a ground layer are previously-formed copper plates, and the signal layer comprises a lead frame. The Official Action also states that column 15, lines 27 - 31 of Miyahara disclose a solder layer formed on an electroplated layer, but the cited passage in fact describes a paste of a brazing material applied to an aluminum nitride substrate 54, and is not a solder layer on an electroplated layer, and certainly not a hot dip solder plating layer atop an electroplated layer as set forth in independent claims 16 and 20.

Therefore, as Miyahara does not disclose a hot dip solder plating layer on an electroplated layer, it does not disclose all the features of claims 16 or 20 and cannot anticipate these claims or claims 17 - 19, 21 - 24, 31, 43, and 44 which depend therefrom. These claims are thus allowable.

Claims 17, 21, and 44 further patentably distinguish the present invention from Miyahara. These claims state that a difficult to solder material on which an electroplated layer is formed is a Fe-Ni alloy. Miyahara does not disclose this feature. In column 7, lines 41 - 47, Miyahara does in fact disclose that the signal layer may be a Fe-Ni alloy, but since there is neither an electroplated layer nor a hot dip solder plating layer on the signal layer, the mere fact that the signal layer can be a Fe-Ni alloy does not result in all the features of

claims 17, 21, and 44 and so cannot anticipate these claims.

Claims 19 and 23 further patentably distinguish the present invention from Miyahara. These claims state that the electroplated layer is a Sn-Ag alloy. Although the Official Action states that column 8, lines 51 - 67 of Miyahara teach that the solder or solderable material may be a Sn-Ag alloy, the Applicant can find no mention of an Sn-Ag alloy in the passage cited by the Official Action, and in any event, the material being discussed in this passage is an adhesive, not an electroplated layer such as is being described by claims 19 and 23. Accordingly, Miyahara does not anticipate these claims.

Claims 24, 43, and 44 further patentably distinguish the present invention from Miyahara These claims state that the portion to be soldered of claim 20 is a lid of a packaged electronic part. The Official Action incorrectly states that Miyahara teaches a lid as a solder coated material. While Miyahara does disclose a package for a semiconductor device 32 which includes a cap 43, the cap 43 bears no resemblance to the structure set forth in claims 20 from which claims 24, 43, and 44 depend. Namely, the cap 43 includes neither an electroplated layer nor a hot dip solder plating layer. As described in column 21, lines 45 - 55 of Miyahara, in the embodiment of Figure 14, for example, the cap 43 comprises aluminum which is joined to the signal layer (lead frame) 53 by an epoxy adhesive as a sealing layer. Thus, as the structure of the cap 43 is totally different from that of the lids set forth in claims 24, 43, and 44 and does not include all the features of these claims, they are not

anticipated by Miyahara.

Rejection 6

In paragraph 6 of the Official Action, claims 16, 18, 20, 22, 25, 28, 34, 39, and 40 were rejected under 35 USC 102(b) as anticipated by Ohno (U.S. Patent No. 4,666,078). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer, and independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. Ohno does not disclose such products or such a method.

Ohno teaches a liquid crystal display panel having terminals comprising an electroless plated layer on a substrate, and a solder layer, which may be formed by immersion in a solder bath, is formed atop the electroless plated layer. The only method of plating which Ohno discloses is electroless plating, and in fact electroplating would be impossible on the substrates employed in Ohno.

Thus, as Ohno does not disclose a hot dip solder plating layer on an electroplated layer, it does not disclose all the features of claims 16, 20, or 25 and cannot anticipate these claims or claims 18, 22, 28, 34, 39, and 40 which depend therefrom. These claims are thus allowable.

Rejection 7

In paragraph 7 of the Official Action, claims 16, 18, 20, 22, 25, 28, 30, 34, 39, and 40 were rejected under 35 USC 102(e) as anticipated by Powell et al (U.S. Patent No. 6,160,310, referred to below as Powell). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer, and independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. Powell does not disclose such products or such a method.

Powell discloses a thin film flexible interconnect for connecting between different substrates. As shown in Figure 1, in one embodiment, a via 11 is formed through a polyimide film 9 down to a lead pattern 7, and metallization 13 is formed on the via 11 by plating. A Cu layer 14 may be plated atop the metallization 13, and a solder layer 15 may be formed atop the Cu layer by plating or wave soldering. Although the metallization 13 and Cu layer 14 may be formed by plating, there is no disclosure of their being formed by electroplating. Furthermore, there is no disclosure of the thickness of the metallization 13, while the thickness of the Cu layer 14 is 12 $\mu$m, which is outside of the range of the electroplated layers set forth in claims 16 and 20.

The Official Action states that column 5, lines 18 - 25 disclose electroplating a layer of excellent solderability such as Ni or Au to a thickness of 2 - 12 μm. This statement is incorrect in that there is no disclosure or suggestion in Powell of electroplating, and the statement is also not pertinent because a plated layer of Au with a thickness of 3 - 12 micrometers referred to in column 5, lines 20 is not a layer on which a solder layer is formed, but is a replacement for a solder bump, to be used for wire bonding. This is clear from column 9, lines 8 - 11 of Powell, which state that a pad of aluminum or gold (the two materials discussed in column 5, lines 18 - 22) can be used as a thin metal pad to replace a solder pad.

Thus, as Powell does not disclose a hot dip solder plating layer on an electroplated layer, it does not disclose all the features of claims 16, 20, or 25 and cannot anticipate these claims or claims 18, 22, 28, 30, 34, 39, and 40 which depend therefrom. These claims are thus allowable.

Rejection 8

In paragraph 8 of the Official Action, claims 16 - 18, 20 - 22, 24, 25, 27, 28, 31, 34, 36, 39, 41, 42, 44, 46, and 48 were rejected under 35 USC 102(b) as anticipated by Geschwind (U.S. Patent No. 4,331,258). This rejection is respectfully traversed.

As described above, independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer, independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an

electroplated layer, and independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath, while independent claim 41 describes a method of forming a packaged electronic part by performing reflow soldering of a lid having a hot dip solder plating layer on an electroplated layer. Geschwind does not disclose such products or methods.

Geschwind discloses a sealing cover for a hermetically sealed container having a lid 12 made of an electrically resistant material, a metal plate "picture frame" on the circumference of one side and the edges of the lid, and a solder ring 16 adherent to and covering the picture frame. The solder ring may be formed by dip coating. Although it is disclosed that the picture frame may be created by selective metal plating, it is not disclosed in Geschwind which of various plating methods (electroplating, electroless plating, mechanical plating) is intended by Geschwind, and the term electroplating appears nowhere in the disclosure of Geschwind. Thus, Geschwind fails to disclose a hot dip solder plating layer on an electroplated layer, so it does not disclose all the features of claims 16, 20, 25, or 41 and cannot anticipate these claims or claims 17, 18, 21, 22, 24, 27, 28, 31, 34, 36, 39, 42, 44, 46, and 48 which depend therefrom. These claims are thus allowable.

Claims 17, 21, 27, 44, 46, and 48 further patentably distinguish the present invention from Geschwind. These claims recite an iron-nickel alloy as a material subjected to electroplating and then hot dip solder plating. Geschwind states

in column 4, lines 12 - 15, "Of the metals/alloys in Table 1, the first eight are potentially acceptable as a material for the lid, while Invar, Kovar, and Alloy 42 do not possess the necessary environmental resistance." Thus, Geschwind specifically rules out the use of a Fe-Ni alloy as a material for treatment and so does not anticipate claims 17, 21, 27, 44, 46, and 48.

Paragraph 15 of the Official Action describes Geschwind as teaching that Kovar and Alloy 42 are suitable materials for use as the lid of Geschwind, but this is not a reasonable interpretation of the language in column 4, lines 12 - 15 that "Of the metals/alloy in Table 1, the first eight are potentially acceptable as a material for the lid, while Invar, Kovar, and Alloy 42 do not possess the necessary environmental resistance." This is a clear statement that Invar, Kovar, and Alloy 42 are <u>not</u> acceptable materials, and if a reference teaches <u>not</u> to use a material, the reference cannot be characterized as simultaneously teaching the use of the material. Paragraph 15 also states that since stainless steel is one of the potentially acceptable materials listed in Table 1 of Geschwind, then Geschwind teaches the use of a material containing Fe and Ni. However, claims 17, 21, 27, 44, 46, and 48 do not read "a material containing Fe and Ni" but rather pertain to use of an iron-nickel alloy. No person skilled in the art would refer to a stainless steel as being an "iron-nickel alloy". Rather, this term is used to refer to a material such as Kovar or Alloy 42 primarily comprising Fe and Ni. An example of the standard usage of this term is found in column 7, line 43 of Miyahara (cited in Rejection 5), which

states "As specific examples, there can preferably be mentioned Fe-Ni alloys (e.g. 42% Ni-remainder of Fe)".

Rejection 9

In paragraph 9 of the Official Action, claims 16 - 18, 20 - 22, 24, 31, 34, and 44 were rejected under 35 USC 102(b) as anticipated by Nagashima et al (U.S. Patent No. Re. 34,484, referred to below as Nagashima). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer with a thickness of 10 - 50 $\mu$m on an electroplated layer, and independent claim 20 describes a portion to be soldered including a hot dip solder plating layer with a thickness of 10 - 50 $\mu$m on an electroplated layer. Nagashima does not disclose any of these products or methods.

Nagashima describes gold-plated electronic components in which a plated layer of an alloy of nickel and cobalt is applied to a metal surface as an undercoat, and then a gold plated layer is formed atop the undercoat. Thus, the products disclosed by Nagashima are not solder coated materials at all but are gold-plated members each having gold as its outermost layer.

Column 4, lines 29 - 33 of Nagashima describe a solderability test according to MIL STD 883-2003 in which leads of undisclosed structure are subjected to dipping in solder in order to test the wettability of the material to solder. This is no more than a test, and Nagashima nowhere discloses a product in

which an electroplated layer has a hot dip solder plating layer. Furthermore, Nagashima contains no disclosure of the thickness of the solder resulting from hot dipping. The Official Action, referring to column 4, lines 17 - 20 of Nagashima, states that the solder in the soldering test has a thickness of about 50 μm. However, the value of 50μm in column 4, lines 17 - 20 refers to the thickness of a solder preform ("A 1.0 t Kovar cap ... was sealed in a hydrogen furnace at 300° C. for 6 minutes using a 50μ thick 80Au/20Sn preform") and has no relationship or relevance to the solderability test described in column 4, lines 29 - 33 of Nagashima.

Thus, Nagashima does not disclose a hot dip plating layer having a thickness of 10 - 50μm as set forth in claims 16 and 20, so it cannot anticipate these claims or claims 17, 18, 21, 22, 24, 31, 34, and 44 which depend therefrom.

Rejection 10

In paragraph 10 of the Official Action, claims 25, 27, 28, and 30 were rejected under 35 USC 103(a) as unpatentable over Sherry (U.S. Patent No. 4,763,829) in view of Svendsen et al (U.S. Patent No. 5,262,718, referred to below as Svendsen). This rejection is respectfully traversed.

Independent claim 25 describes a method including electroplating a difficult to solder material and then passing the difficult to solder material through a solder bath. Neither of the cited references discloses or suggests such a method.

Sherry discloses a method of soldering electronic components

in which bonding pads 11 - 13 are formed on the surface of a silicon chip 10, and then the chip 10 is exposed to solder by dipping a wafer 40 (which is to be formed into chips) in solder to form solder mounds 15 - 17 atop the bonding pads. Sherry does not disclose how the bonding pads are formed and nowhere suggests forming them by electroplating.

Svendsen discloses a uniaxially conductive sheet comprising a porous insulating sheet having pores formed therein. The sheet is electrolessly plated with a first layer of material in the pores, and the plated material is removed from the major surfaces of the sheet to isolate the pores from one another. Further plating is performed atop the plated pore surfaces to fill the pores and/or to make the plating project beyond the surface of the sheet. The pores may then be filled with solder by wave soldering or capillary absorption.

Column 4, lines 40 - 41 of Svendsen do mention the possibility of performing electroplating, but this electroplating is only performed atop a previously formed electrolessly plated layer of a material having excellent solderability (Ni, Cu, Ag, Au, etc., as set forth in column 2, lines 40 - 42). There is no suggestion in Svendsen of performing electroplating on a substrate of a difficult to solder material as set forth in claim 25.

Therefore, as neither of the references discloses or suggests electroplating a difficult to solder material, they do not contain sufficient teachings that could be combined so as to result in all the steps set forth in claim 25 and so cannot

render this claim obvious. Claim 25 and claims 27, 28, and 30 which depend from it are therefore allowable.

Rejection 11

In paragraph 11 of the Official Action, claims 24, 31, 33, 35, 36, 38, and 41 - 48 were rejected under 35 USC 103(a) as unpatentable over McAndrew in view of Bartley et al (U.S. Patent No. 6,084,775, referred to below as Bartley). This rejection is respectfully traversed.

Claims 24, 43, and 44 describe a portion to be soldered of an electronic part which is a lid of a packaged electronic part. Claims 36, 45, and 46 describe a method of manufacturing a solder coated material in which a difficult to solder material forms part of a lid of a packaged electronic part. Claims 41, 42, 47, and 48 describe a method of forming a packaged electronic part including performing reflow soldering of a lid to join the lid to a package. Claim 31 describes a portion to be soldered of an electronic part which is a lead frame, and claim 35 describes a soldering method for a lead frame. Furthermore, claim 33 describes a portion to be soldered of an electronic part which is a shield of a module, and claim 38 describes a soldering method for a part of a shield of module. In each of these claims, the lid, the lead frame, or the shield of a module has an electroplated layer and a hot dip solder plating layer formed thereon. Neither of the cited references discloses or suggests such an arrangement or method, because neither of the references relates to a lid of a packaged electronic part, a lead frame, or

a shield of a module.

As described above with respect to Rejection 1, McAndrew relates to a method of assembling electronics on a printed wiring board. There is no disclosure in McAndrew concerning a lid, a lead frame, or a shield of a module as in claims 24, 31, 33, 35, 36, 38, and 41 - 48.

Bartley discloses a method of attaching an aluminum heat sink to an IC module. A solderable layer is plated on the base 43 of a heat sink 41, and then a solder release layer 47 comprising a solder alloy is applied atop the plating by a suitable method, such as wave soldering. The heat sink 41 is then attached to an IC module or chip 51 with a mechanically compliant, thermally conductive adhesive 55. If the heat sink 41 needs to be removed from the module 51, heat is applied to the release layer 47 to liquify it, thereby enabling the heat sink 41 to be easily detached from the module 51. Bartley has no relationship to either lids of packaged electronic parts, to lead frames, or to shields of modules. It is not even related to soldering, since the solder release layer 47 is not used to solder the heat sink 41 to another member but only to permit the detachment of the heat sink 41 from the adhesive 55.

Accordingly, as neither of the cited references teaches a lid of a packaged electronic part, a lead frame, or a shield of a module, the references do not contain teachings that could be combined to result in all the features set forth in claims 24, 31, 33, 35, 36, 38, and 41 - 48 and so cannot render these claims obvious. These claims are thus allowable.

Rejection 12

In paragraph 12 of the Official Action, claims 32 and 37 were rejected under 35 USC 103(a) as unpatentable over Ohno in view of Potega (U.S. Patent No. 6,152,597). This rejection is respectfully traversed.

Claim 32, which depends from claim 20, describes a portion to be soldered of an electronic part having an electroplated layer and a hot dip solder plating layer which is a battery terminal, while claim 37, which depends from claim 25, describes a method of manufacturing a solder coated material in which a difficult to solder material which is electroplated and then dip soldered form part of a battery terminal. Neither of the cited references discloses or suggests such an arrangement or method.

As discussed above with respect to Rejection 6, Ohno discloses a liquid crystal display having terminals comprising an electroless plated layer on a substrate, and a solder layer, which may be formed by immersion in a solder bath, is formed atop the electroless plated layer. Ohno contain no teachings concerning a battery terminal.

Potega discloses a flexible thermistor assembly which can be wrapped around an existing battery pack. There is no disclosure in Potega of the electrodes of the battery pack having any particular structure, let alone of their comprising a difficult to solder material having an electroplated layer and a hot dip solder plating layer as in claims 32 and 37. The Official Action cites column 6, lines 36 - 46 and column 6, lines 66 - column 7, line 2 as supposedly teaching terminals of a battery cell which

are plated and then wave soldered, but the passage cited by the Official Action describes not a battery electrode but an electrode of a so-called PTC thermistor for wrapping around a conventional battery cell, such as that described by the patent which Potega refers to as Friel (U.S. Patent No. 4,882,466).

Thus, as neither of the cited references discloses or suggests a battery terminal having an electroplated layer and a hot dip solder plating layer, the references do not contain teachings that could be combined to result in all the features set forth in claims 32 or 37 and so cannot render them obvious. Claims 32 and 37 are therefore allowable.

Rejection 13

In paragraph 13 of the Official Action, claims 49 - 52 were rejected under 35 USC 103(a) as unpatentable over Geschwind in view of Sugihara et al (US 2001/0052643 A1, referred to below as Sugihara). This rejection is respectfully traversed because there is no motivation in the references to combine them in the manner proposed in the Official Action.

Geschwind discloses a sealing cover which is formed by stamping or otherwise cutting a metal sheet into the shape of a lid 12. A solderable area is created on the lid 12 by selective plating of a picture frame 14 on the circumference of one side and edges of the lid 12, and then a solder ring 16 is adhered to the picture frame 14. The lid 12 can be attached to a semiconductor package 20 by heating the lid 12 and the package 20 to melt the solder 16 and form a seal to a metallic sealing ring

40 of the package 20. It is desirable to have the soldering 16 form a picture frame 14 covering the edges of the lid 12 so as to form an external solder fillet 42 to permit visual observation of the adequacy of a seal.

Sugihara discloses a semiconductor device having outer leads 2 which are plated with solder plating 3 to improve the soldering characteristics of the leads 2. A depression 11 is formed in a lead either before or after plating, and the lead 2 is cut through at the depression 11 so that the solder plate 3 is present on an end surface of the lead 1 over a portion of its height. The plating 3 on the end surface increases the wettability of the end surface and causes a solder fillet 4 to rise up higher during soldering than it would in the absence of the solder plating 3.

The Official Action proposes to modify the sealing cover of Geschwind to punch the lid 12 after plating is carried out. The reason which the Official Action gives for the proposed modification is that doing so would form the lid into a required shape in a simple and cost effective manner.

However, neither the Official Action nor the references show that such a modification of Geschwind would be any simpler or cost effective than the method that Geschwind already uses. In Sugihara, punching has to be carried out after plating because, as stated in paragraph 0009 of Sugihara, the leads to be plated must extend past the portions to be cut in order to provide an electrical connection to the lead frame during plating. In contrast, punching a sheet to form a lid prior to plating is not

an impediment to plating in the case of Geschwind, and in fact is desirable, since it enables solder to be formed over the entire surface of the outer edges of the lid.

Thus, since the references provide no motivation for the modification of Geschwind proposed in the Official Action, the rejection of claims 49 - 52 does not set forth a prima facie case of obviousness and is therefore improper. Claims 49 - 52 are accordingly allowable.

In light of the foregoing remarks, it is believed that the present application is in condition for allowance, and favorable consideration is respectfully requested.

Respectfully submitted,

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PATENT

In re application of:

MITSUO ZEN

Serial No.: 09/868,573 Art Unit: 1725

Filed: August 20, 2001 Examiner: L. Edmondson

For: SOLDER COATED MATERIAL AND METHOD FOR ITS MANUFACTURE



Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

A reponse in the above-identified patent application is attached.

[X] No additional claim fee is required.

| | (Col. 1) | | (Col. 2) | (Col. 3) | SMALL ENTITY | | OTHER THAN A SMALL ENTITY | |
|---|---|---|---|---|---|---|---|---|
| /////// | CLAIMS REMAINING AFTER AMENDMENT | ///// | HIGHEST NO. PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE | ADDIT. FEE | RATE | ADDIT. FEE |
| TOTAL | * 37 | MINUS | ** 37 | = 0 | x 9= | $ | x 18= | $0 |
| INDEP | * 4 | MINUS | *** 4 | = 0 | x42= | $ | x 84= | $0 |
| FIRST PRESENTATION OF MULT. DEP. CLAIM | | | | | +140 | $ | +280= | $ |
| | | | | | TOTAL | $ | TOTAL | $0 |

* If entry in Col. 1 is less than that in Col. 2, write "0" in Col. 3.
** If the highest no. previously paid for IN THIS SPACE is less than 20, write "20" in this space.
*** If the highest no. previously paid for IN THIS SPACE is less than 3, write "3" in this space.

[ ] Please charge Deposit Account No. 50-1079 in the amount of $.

[ ] A check in the amount of $ is attached in payment of the extra claim fee.

[ ] The Commissioner is authorized to charge any deficiency in the following fees associated with this communication and to credit any excess payment to Deposit Account No. 50-1079. A duplicate copy of this letter is attached.

[ ] Any filing fees pursuant to 37 CFR §1.16 for the presentation of extra claims.

[ ] Any patent application processing fees pursuant to 37 CFR §1.17, including extension of time fees pursuant to 37 CFR §1.17(a)-(d).

Respectfully submitted,

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